UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/630,615	07/30/2003	Josey G. Angilivelil	TI-34945	8686

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TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER
DOAN, NGHIA M

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 12/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No.	Applicant(s)
	10/630,615	ANGILIVELIL, JOSEY G.
	Examiner	Art Unit	
	Nghia M. Doan	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _07/30/2003_.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-28_ is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-11, 13-21, and 23-28_ is/are rejected.

7)☒ Claim(s) _12 and 22_ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _30 July 2003_ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some *   c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)   Paper No(s)/Mail Date _07/30/2003_.

4)☐ Interview Summary (PTO-413)   Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

1.   Responsive to communication application 10/630,615 filed on 07/30/2003,

claims 1-28 are pending.

Claim Rejections - 35 USC § 102

2.   The following is a quotation of the appropriate paragraphs of 35

U.S.C. 102 that form the basis for the rejections under this section made in this

Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3.   **Claims 1-8, 13-18, 23-25 and 27-28 are rejected under 35 U.S.C. 102(e)**

as being anticipated by Grundmann et al (Grundmann) (US 6,327,686).

4.   **With respecive to claim 1**, Grundmann discloses a method to facilitate

evaluating an integrated circuit (1C) chip (col. 5, ll. 10-19) comprising:

determining a set of critical paths (the critical path identifier (CPI)) for a

design associated with the IC chip, at least some of the critical paths being

determined based on timing characteristics thereof (col. 2, ll. 16-27, col. 3, ll. 5-

17, col. 4, ll. 5-18, and col. 7, ll. 1-20);

generating a plurality of sets of timing test patterns for the set of critical

paths, each set being generated according to desired performance criteria (col.

2, ll. 27-41, col. 7, ll. 56-67 and col. 8, ll. 1-23); and

applying (inserting) at least one of the plurality of sets of test patterns to the IC chip to provide corresponding test data indicative of performance-related characteristics of the IC chip (col. 2, ll. 48-55, col. 5, ll. 5-9, fig. 4, col. 8, ll. 10-23).

5.   **With respective to claim 2**, Grundmann discloses the method of claim 1, the timing characteristics including a timing threshold indicative of slack between endpoints (fig. 1, col. 4, ll. 5-18) of an associated path of the design associated with the IC chip, the set of critical paths including data paths of the design associated with the IC chip having a slack (delay) less than that defined by the timing threshold (the time need for the signal traverse combination logic element would greater than the clock speed would allow for correct logic propagation) (fig. 1, col. 6, ll. 21-36).

6.   **With respective to claim 3**, Grundmann discloses The method of claim 1, the determination of the set of critical paths further comprising performing static timing analysis on the design associated with the IC chip to provide slack characteristics for paths of the design associated with the IC chip (col. 2, ll. 16-27, and ll. 46-59).

7.   **With respective to claim 4**, Grundmann discloses the method of claim 3, the determination of the set of critical paths further comprising:

defining the timing characteristics as a slack limit (fig. 1, col. 6, ll. 12-20); and

identifying the critical paths (the critical path identifier (CPI)) of the design associated with the IC chip based on a comparison (evaluation) of the slack limit

relative to the slack characteristics (edge detector) provided by the static timing analysis for paths of the design associated with the IC chip (fig. 1, col. 6, ll. 21-30 and col. 7, ll. 1-34).

8.   **With respective to claim 5**, Grundmann discloses the method of claim 1, the desired performance criteria (proper circuit operation) of each set of the test patterns further comprising a target speed related characteristic (meet its clocking frequency requirements) (col. 1, ll. 50-58 and col. 4, ll. 5-8).

9.   **With respective to claim 6**, Grundmann discloses the method of claim 1, further comprising grading a performance characteristic of the IC chip based on the test data for at least one set of the plurality of sets of test patterns (col. 5, ll. 8-17, col. 7, ll. 15-20, fig. 5, col. 7, ll. 56-65).

10.   **With respective to claim 7**, Grundmann discloses the method of claim 1, the application of the at least one of the plurality of sets of test patterns further comprising:

applying a first set of the plurality of test patterns to the IC chip, the desired performance criteria associated with the first set of test patterns defining a first associated performance level for the IC chip (col. 5, ll. 1-9, col. 8, ll. 25-55); and

ascertaining whether the IC chip meets the first associated performance level based on the corresponding test data (col. 7, ll. 61-63).

11.   **With respective to claim 8**, Grundmann discloses the method of claim 7, the application of the plurality of sets of test patterns further comprising:

if the IC chip fails the first associated performance criteria, applying at least one other set of the plurality of sets of test patterns to the IC chip, the desired performance criteria associated with the at least one other set of test patterns defining a second associated performance level for the IC chip (col. 7, ll. 60-61, col. 8, ll. 10-23, and ll. 56-63, -- modifying the previous test pattern and produced new set of test patterns --); and

ascertaining whether the IC chip meets the second associated performance level based on the corresponding test data (col. 8, ll. 20-23).

12.   **With respective to claim 13**, Grundmann discloses the method of claim 1, further comprising:

evaluating the test data for the plurality of sets of test patterns to ascertain an indication of process variations associated with the fabrication of the IC chip (col. 5, ll. 10-19, col. 2, ll. 26-33); and

employing the indication of process variations to adjust process parameters for subsequent fabrication of IC chips based on the design associated with the IC chip (col. 1, ll. 62-67, col. 2, ll. 1-15, and col. 5, ll. 10-19) .

13.   **With respective to claim 14**, Grundmann discloses the method of claim 1, further comprising evaluating the test data generated for each set of the plurality timing patterns to identify performance capabilities of the IC chip (fig. 3, col. 7, ll. 10-36).

14.   **With respective to claim 15**, Grundmann discloses a computer-implemented method to determine performance-related characteristics of an integrated circuit (IC) chip (fig. 4, see its description), the method comprising:

applying a first set of test patterns of a plurality of sets of test patterns to the IC chip (col. 2, II. 48-55, col. 5, II. 5-9, fig. 4, col. 8, II. 10-23), the plurality of test patterns being generated for a subset of critical paths of the IC chip based on timing characteristics of the subset of critical paths (col. 2, II. 27-41, col. 7, II. 56-67 and col. 8, II. 1-23) ascertained (determined) from timing analysis of a design for the IC chip (col. 2, II. 16-27, col. 3, II. 5-17, col. 4, II. 5-18, and col. 7, II. 1-20);

storing test data based on the application of the first set of test patterns (col. 7, II. 39-40);

repeating the application and the storing for each other set of test patterns of the plurality of test patterns (fig. 5, col. 8, II. 10-23); and

evaluating the stored test data for the IC chip for at least one of the plurality of sets of test patterns to provide an indication of at least one of performance-related characteristic of the IC chip (col. 5, II. 10-19 and col. 8, II. 25-63).

15.   **With respective to claim 16**, Grundmann discloses the method of claim 15, the timing characteristics is a timing threshold indicative of slack between endpoints (fig. 1, col. 4, II. 5-18) of an associated path of the design of the IC chip, the subset of critical paths including data paths having a slack (delay) less than that defined by the timing threshold (the time need for the signal traverse combination logic element would greater than the clock speed would allow for correct logic propagation) (fig. 1, col. 6, II. 21-36).

16.   **With respective to claim 17**, Grundmann discloses the method of claim

15, each set of plurality of sets of test patterns further being generated for a

target operating speed related characteristic (col. 2, ll. 16-27, and ll. 46-59).

17.   **With respective to claim 18**, Grundmann discloses the method of claim

15, further comprising grading a performance characteristic of the IC chip based

on the stored test data for at least one set of the plurality of sets of test patterns

(col. 7, ll. 39-40, col. 5, ll. 10-19 and col. 8, ll. 25-63).

18.   **With respective to claim 23**, Grundmann discloses the method of claim

15, further comprising:

        the evaluation of the stored test data further comprising evaluating the

stored test to ascertain an indication of process variations associated with the

fabrication of the IC chip (col. 5, ll. 10-19 and col. 8, ll. 25-63).; and

        employing the indication of process variations to adjust process

parameters for subsequent fabrication of IC chips based on the design of the IC

chip (col. 1, ll. 62-67, col. 2, ll. 1-15, and col. 5, ll. 10-19).

19.   **With respective to claim 24**, Grundmann discloses a system (fig. 4, see

its description) to facilitate evaluating performance of an integrated circuit chip,

comprising:

        means for identifying a set of critical paths (the critical path identifier (CPI))

of the IC chip based on timing margins associated with at least some paths of the

set of critical paths (col. 2, ll. 16-27, col. 3, ll. 5-17, col. 4, ll. 5-18, and col. 7, ll. 1-

20);

means for generating test patterns for the set of critical paths of the IC

chip based on a plurality of target performance criteria (col. 2, ll. 27-41, col. 7, ll.

56-67 and col. 8, ll. 1-23); and

means for applying the test patterns to the IC chip to generate test data

indicative of performance for the IC chip (col. 2, ll. 48-55, col. 5, ll. 5-9, fig. 4, col.

8, ll. 10-23).

20.   **With respective to claim 25**, Grundmann discloses the system of claim

24, further comprising means for defining different (greater than) desired target

performance criteria for each of a plurality of sets of test patterns (the time need

for the signal traverse combination logic element would greater than the clock

speed would allow for correct logic propagation) (fig. 1, col. 6, ll. 21-36).

21.   **With respective to claim 27**, Grundmann discloses the system of claim

24, further comprising means for ascertaining (determining) an indication of

process variations associated with fabrication of the IC chip based on the test

data (col. 5, ll. 8-17, col. 7, ll. 15-20, fig. 5, col. 7, ll. 56-65).

22.   **With respective to claim 28**, Grundmann discloses the system of claim

24, further comprising means for ascertaining (determining) an indication of

operating speed performance (meet its clocking frequency requirements)

associated with fabrication of the IC chip based on the test data (col. 1, ll. 50-58

and col. 4, ll. 5-8).

Claim Rejections - 35 USC § 103

23.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for

all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

24.   **Claims 9-11, 19-21 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Grundmann et al (Grundmann) (US 6,327,686) in view of Ramon (US 6,184,048).**

25.   **With respective to claim 9-11, 19-21 and 26**, Grundmann discloses all the limitation of the set forth claims as rejection under 35 U.S.C 102 (e).

Grundmann does not explicitly discloses (claims 9, 19 and 26) applying a stress to the IC chip at least one of before or after the application of the at least one of the plurality of sets of test patterns; (claims 10, 20, and 26) determining an impact on performance of the IC chip associated with the application of stress to the IC chip; and (claims 11 and 21) determination of the impact on performance of the IC chip further comprising determining an impact on speed degradation of the IC chip associated with the application of stress to the IC chip.

Ramon discloses (claims 9, 19 and 26) applying a stress to the IC chip at least one of before or after the application of the at least one of the plurality of sets of test patterns (Ramon, col. 9, ll. 14-20, fig. 10 and see description); (claims 10, 20, and 26) determining an impact on performance of the IC chip associated with the application of stress to the IC chip (Ramon, fig. 7, and col. 12-25); and (claims 11 and 21) determination of the impact on performance of the IC chip further comprising determining an impact on speed degradation (critical delay

path) of the IC chip associated with the application of stress to the IC chip

(Ramon, fig. 9, and col. 10, ll. 36-42).

It would have been obvious to one of ordinary skill in the art to combine

Grundmann and Ramon because Ramon discloses the detail of burn-in testing

(Grundmann, col. 1, ll. 26-30) through the used of stress test (Ramon, col. 6, ll.

45-57) which is required to achieve IC's that meet specifications for speed, power

consumption, and operational margins.

Allowable Subject Matter

26.   Claims 12 and 22 are objected to as being dependent upon a rejected

base claim, but would be allowable if rewritten in independent form including all

of the limitations of the base claim and any intervening claims.

27.   The following is a statement of reasons for the indication of allowable

subject matter: the Grundmann and Ramon references do not fairly teach or

suggest "identifying a location on the IC chip impacted by the application of

stress to the IC chip and at least one potential process parameter capable of

causing a defect at the location during fabrication of the IC chip".

Conclusion

Any inquiry concerning this communication or earlier communications from

the examiner should be directed to Nghia M. Doan whose telephone number is

571-272-5973. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the

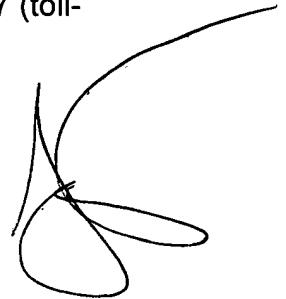examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax

phone number for the organization where this application or proceeding is

assigned is 571-273-8300.

Information regarding the status of an application may be obtained from

the Patent Application Information Retrieval (PAIR) system. Status information

for published applications may be obtained from either Private PAIR or Public

PAIR. Status information for unpublished applications is available through

Private PAIR only. For more information about the PAIR system, see http://pair-

direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-

free).

A. M. Thompson
Primary Examiner
Technology Center 2800

Nghia M. Doan
Patent Examiner
AU 2825
NMD